Accredited by NAAC & NBA*

SVCE BENGALURU

SRI VENKATESHWARA COLLEGE OF ENGINEERING

— Affiliated to VTU, Approved by AICTE, Recognised by UGC u/s 2(f) & 12(B)—

EXAMINATION SECTION

IMPLEMENTATION OF EXAMINATION REFORMS

Sri Venkateshwara College of Engineering is affiliated to Visvesvaraya Technological University- Belagavi. The SEE exams are conducted as per the guidelines of the university and the question paper setting and valuation is done at university level. The following reforms are implemented in CIE conduction to ensure implementation of AICTE Examination reforms.

I. Bloom's Taxonomy for Assessment Design

1) Internal Assessment question papers are set with 30% question in Understand Level, 40% in Apply Level and 30% in Analyze level.
2) **IA Question Paper Moderation:** Question papers will be allocated to moderators for scrutiny. The moderators are selected based on subject proficiency. Moderators scrutinize the question papers with respect to quality, knowledge level distribution and format.
3) **Moderation of IA Answer scripts:** For each subject two randomly picked IA scripts will be evaluated by moderator to ensure the uniformity in evaluation. This will ensure the uniformity in evaluation methods.
4) **Higher order thinking Questions:** HoT questions are given as assignment to students to encourage students to think beyond literal questions and to promote critical thinking skills.
5) **Learning Outcome weightage:** The CIE question papers are set such that all learning outcomes are uniformly covered. Three CIE are planned at

uniform intervals as per university guidelines and the question papers are designed such that equal weightage is given to all learning outcomes.

2018 and 2021 Scheme

Test/Cos	CO1	CO2	CO3	CO4	CO5
CIE-1	30	20			
CIE-2		10	30	10	
CIE-3				20	30

2022 Scheme

Test/Cos	CO1	CO2	CO3	CO4	CO5
CIE-1	20	20	10		
CIE-2			10	20	20

6) At least 2 Quiz/Course is conducted which promotes self-assessment and makes learning more effective.
7) Open ended problems are given as team activity to trigger critical thinking of students.
8) Video Assignments are given to students to improve their communication skills.
9) Moderation Committee is formed to review the question bank developed by faculty to review and ensure the quality of questions.

II. Open-Book Examinations

Open book CIE is conducted in selected subjects to emphasize more on problem-solving, application of knowledge and higher-order thinking rather.

III. QUESTION PAPER DELIVERY SYSTEM FOR CIE.

The CIE question papers are generated using a Digital Question Paper Delivery System. In this deterministic model, the professor's will be uploading the Moderated question bank by considering the following parameters like Course Outcomes, Knowledge Level, Marks, Complexity of the questions like Easy, Moderate and Difficult. Based on these parameters the deterministic model is defined according to generate the question paper. The preference will be decided by the college, and it will be monitored once in a while to improvise the student to go to next level.

Advantages:

a. Outcome Based Education concept is implemented (Student Centric Approach)
b. Faculty can concentrate on Research activities by reducing time for mundane tasks like questions preparation, Scheme Preparation etc., (Once entered data can be used multiple number of times)
c. Quality of education will improve.

There are other benefits as well for both professors and students.

- Professors can make use it for surprise tests and Slip Tests.
- Repetitive number of tests can be conducted to improve the student Performance.

Principal
Dr. NAGESWARA GUPTHA M.
PRINCIPAL
Sri Venkateshwara College of Engineering
Vidyanagar, Bangalore-562 157

MODERATION PROCESS

Internal Quality Assurance Cell

Ref: SVCE/IQAC/2023 – 24/ **Date:** 05/12/2023

CIRCULAR

As per the discussion in the IQAC Committee meeting, all the HoD's are request to form the Moderation / Review Committee in the department level to review / Moderate the CIE Process.

Guidelines for Moderation / Review Committee formation:

1. The Chairman of the committee will be the Head of the department.
2. Two senior faculty members (Minimum 5 Years of Experience) nominated by Principal / HoD as members of the committee.

Roles and Responsibilities of the Moderation / Review Committee:

Steps for Question Bank Moderation:

1. Collection of Question Bank from all the course teachers for all the courses before uploading the questions to the QPDS system.
2. Moderation of questions in the question bank as per the Annexure – I.
3. Correction in the question bank by the course teacher, if any as per the recommendation of moderation committee.
4. Uploading the questions in QPDS system by the course teacher.
5. Random verification of correctness of uploaded questions by the committee.

Steps for Moderation of CIE Process:

1. Split-up of marks used for each of the different types of assessment in the course may be checked.
2. Checking of the questions to find whether it maps to course outcomes.
3. Checking the difficulty level of questions paper ie, is the difficulty level on the high extreme, very easy or otherwise.
4. Whether the assessment modes are used to cover the entire syllabus or not.
5. Checking the manner of awarding the marks, i.e has correction been at the extremes, liberal or tough?
6. Moderation should not be restricted to just assessment but also includes the assessment design (Scheme of Evaluation).

Internal Quality Assurance Cell

7. After the CIE Testes, need to conduct Moderation of CIE process as per the Annexure – II.

Moderation / Review process may be conducted after each test or after the tests in case there is a large number of failures or high marks.

5/12/23
IQAC Coordinator

06/12/2023
CoE

OSDIEC2023
Principal
PRINCIPAL
Sri Venkateshwara College of Engineering
Vidyanagar, Bangalore-562 157

Encl: Annexture 1.

E-Circulation To:

1. HoDs: ECE, CSE, ISE, CSE-AI, CSE-DS, CSE-CY, ME, CE, BS.
2. Dean – Academics, Registrar, COE, Library, Q-RIDES.

Department of _____

Moderation Committee Report

Pre – Examination Audit of Question Bank **AY: 2023 - 2024**

Course Title		**Semester**	
		Course Code	
Name of the Faculty Members			

Sl. No.	Parameters	(Yes / No)
1	Are the questions evenly distributed to cover the syllabus?	
2	Are the questions complete with necessary data / diagrams / constants?	
3	Are the questions unique (i.e. no repetition) in various sections of the question bank?	
4	Whether mapping of CO/RBT and the questions are done properly?	
5	Is Knowledge levels of the questions are distributed as per the course content.	
6	Is the question bank supports Problem solving levels.	
7	Is the question bank has Hot's knowledge levels questions.	
8	How many questions to be corrected in the question bank?	
Remarks:		

Certified that the auditing of the above-mentioned question bank was carried out with the comments listed above. The question bank can be **accepted / rejected.**

Name of the Moderation Committee Members	Designation	Signature with Date

- Draft --

05-DEC-2023

Programme Coordinator

SAMPLE CIRCULAR

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EXAMINATION SECTION

Ref: SVCE/EXAM/2023-24/055 Date: 23/01/2024

CIE and Practical IA for 3rd Sem UG Courses

The II CIE for Second Year UG Courses (III Sem) is scheduled form 13th Feb 2024 ***The Test will be conducted for 100 Marks with 3 hours of duration***

All faculty are informed to prepare the question bank and submit it to Moderation committee. The moderation committee has to complete the process as per the Circular issued by IQAC Cell before ***5th February 2024 (Monday).***

Minimum number of questions to be uploaded

Kx	K2	K3	K4	Total
Full Module	6	6	6	18
Half Module	3	3	3	9

For 2.5 modules minimum number of questions to be uploaded is 45

The Assessments for Practical Courses should be scheduled by respective departments from 29th January to 9th February with the approval of Principal.

NOTE:

1. Duplicate Questions Should be avoided in Question Bank. Question bank must have only Unique Questions.
2. Faculties need not include header details. Header details will be taken care by QPDS team.
3. The template given for question bank should not be modified. Example for Module 1, it should be M1, for Knowledge level K1, K2.
4. Auto Numbering must be avoided.
5. If there are any images in the question bank the resolution should be 3 X 5.5 cms.

All are requested to stick on to the schedule and support in smooth conduction of the QPDS Process.

24/01/2024

Controller of Examinations

Dr. SUNIL. S.
Controller of Examination
Sri Venkateshwara College of Engineering
Vidyanagar, Bengaluru-562 157

24 Jan 2024

Principal

Dr. NAGESWARA GUPTHA M.
PRINCIPAL
Sri Venkateshwara College of Engineering
Vidyanagar, Bangalore-562 157

E-Circulation to
1. HoDs: ECE, CSE, ISE, CA, CY, DS, ME, CE, BS, MBA.
2. Dean – Academics, Registrar, Library, Q-RIDES, IQAC.

SAMPLE QUESTION BANK

<table>
<tr><th>Sl</th><th>Cos</th><th>KLs</th><th>M</th><th>Questions</th><th>Marks</th></tr>
<tr><td>1</td><td>CO1</td><td>K2</td><td>M1</td><td>Explain different functional units of a digital computer.</td><td>10</td></tr>
<tr><td>2</td><td>CO1</td><td>K2</td><td>M1</td><td>What is a stored program concept? Explain the functional units of a stored program digital computer with a block diagram.</td><td>10</td></tr>
<tr><td>3</td><td>CO1</td><td>K2</td><td>M1</td><td>Explain the function of processor registers with a block diagram.</td><td>10</td></tr>
<tr><td>4</td><td>CO1</td><td>K2</td><td>M1</td><td>Explain different functional units of a computer. Mention the function of the processor registers i) PC i) MAR iii) IR .</td><td>10</td></tr>
<tr><td>5</td><td>CO1</td><td>K3</td><td>M1</td><td>Describe and explain the connections between the processor and the main memory.</td><td>10</td></tr>
<tr><td>6</td><td>CO1</td><td>K3</td><td>M1</td><td>Describe the basic operational concepts between the processor and memory.</td><td>10</td></tr>
<tr><td>7</td><td>CO1</td><td>K2</td><td>M1</td><td>Explain with a neat diagram the connection between the processor and the computer memory.</td><td>10</td></tr>
<tr><td>8</td><td>CO1</td><td>K2</td><td>M1</td><td>What is a bus? Explain single bus and multiple bus structure used to interconnect functional units in computer system.</td><td>10</td></tr>
<tr><td>9</td><td>CO1</td><td>K4</td><td>M1</td><td>Assuming that the reference computer is ultra SPARCIO workstation with 300 MH ultra SPARC-IH processor. A company has to purchase 500 new computers hence ordered testing of a new computer with SPEC2000 (run on reference as well as new computer). Following observations were made.
<table>
<tr><th>Programs</th><th>Run time on reference computer</th><th>Run time on new computer</th></tr>
<tr><td>1</td><td>50 minutes</td><td>5 minutes</td></tr>
<tr><td>2</td><td>75 minutes</td><td>4 minutes</td></tr>
<tr><td>3</td><td>60 minutes</td><td>6 minutes</td></tr>
<tr><td>4</td><td>30 minutes</td><td>3 minutes</td></tr>
</table>
The company system manager will place the orders for purchasing new computers only if the overall SPEC rating is at least 12.00. Ater the said test, will the system manager place order the purchase of new computers.</td><td>10</td></tr>
<tr><td>10</td><td>CO1</td><td>K4</td><td>M1</td><td>Program execution time is defined by T=(N*S)/R. Program can be run on RISC or a CISC computer. Both computers use pipelined instruction execution. Effective value of S in T for RISC machine is 1.2 but it is only 1.5 for CISC machine. Both machines have the same clock rate R. Find the value of N on the CISC machine as a percentage of N for the RISC machine. if the time for execution on both machines is the same. Recalculate the ratio of the clock rate R for the RISC machine is 15 % higher than for the CISC</td><td>10</td></tr>
</table>

				Machine.	
11	CO1	K2	M1	Explain the basic performance equation? How to measure the performance of the computer? Explain.	10
12	CO1	K2	M1	What is performance measurement? Explain the overall SPEC rating for the computer in a program suite.	10
13	CO1	K2	M1	With suitable example, explain how performance is measured using SPEC rating and give its significance.	10
14	CO1	K2	M1	What is performance measurement? Explain the overall SPEC rating for the computer in a Program suit.	10
15	CO1	K2	M1	Distinguish between unsigned and signed integers. With examples, indicate when each type of integers will be useful.	10
16	CO1	K2	M1	What is overflow in integer arithmetic? Explain how overflow can be detected, with an illustration.	10
17	CO1	K4	M1	Represent 1259.125_{10} in single precision and double precision formats.	10
18	CO1	K4	M1	Represent - 307.1875_{10} in single precision and double precision formats.	10
19	CO2	K2	M2	What is an addressing mode? Explain different addressing modes.	10
20	CO2	K2	M2	Differentiate addressing modes used to specify the location of operand found in most computers.	10
21	CO2	K2	M2	Explain with examples, all the generic addressing modes, with assembler syntax.	10
22	CO2	K2	M2	What are assembler directives? explain any two directives.	10
23	CO2	K2	M2	What is the function of an assembler directive? Give two examples of assembler directives used for the reservation of memory location for variables? State their functions.	10
24	CO2	K3	M2	Describe and explain flowchart showing operation of assembler during first pass and second pass	10
25	CO2	K2	M2	Explain the operation of stack with an example.	10
26	CO2	K2	M2	What is subroutine linkage. How are parameter are passed to subroutine.	10
27	CO2	K2	M2	Explain the functions to be performed by a typical I/O interface with a typical input or output interface.	10
28	CO2	K4	M2	Aanlyze and Write a program to evaluate the arithmetic statement **Y=(a+b)*(c+d)** using three-address,two-address,one-address and zero address instructions	10
29	CO2	K2	M2	Explain Basic instruction cycle with interrupt	10
30	CO3	K4	M3	Analyze and Design flow chart showing operation of assembler during Second pass?	10
31	CO3	K2	M3	What is Interrupt? With neat diagram explain the concept of	10

				Interrupt	
32	CO3	K4	M3	Develop the hardware mechanism for handling multiple interrupt requests	10
33	CO3	K2	M3	Explain Direct Memory Access(DMA)?	10
34	CO3	K2	M3	Explain Hardware Controlled Data Transfer ?	10
35	CO3	K4	M3	Develop the hardware mechanism for three data transfer modes of DMA	10
36	CO3	K3	M3	Build a distributed arbitration scheme?	10
37	CO3	K3	M3	With neat sketches,explain the various approaches to bus arbitration.	10
38	CO3	K3	M3	With neat sketches,explain the flowchart for I/O services routine.	10
39	CO3	K2	M3	Explain Basic I/O Interfacing Techniques ?	10
40	CO3	K3	M3	With neat sketches,Explain the Single Level Interrupt System.	10

SAMPLE CIE QUESTION PAPER

CBCS SCHEME--2022

1	V	E							

Department of ECE

Continuous Internal Examination I

Course Code: BEC306C **Course Title: Computer Organization and Architecture** **Semester :III**

Date :24-01-2024 **Time : 12:30PM to 2:00PM** **Max. Marks:50**

Instructions: ***Answer One Full Question From each Part***

S.N	Cos	KLs	Questions	Marks
			(PART A)	
1a	CO1	K3	Describe and explain the connections between the processor and the main memory.	10
1b	CO1	K2	Explain the basic performance equation? How to measure the performance of the computer? Explain.	10
			(OR)	
2a	CO1	K2	With suitable example, explain how performance is measured using SPEC rating and give its significance.	10
2b	CO1	K2	Distinguish between unsigned and signed integers. With examples, indicate when each type of integers will be useful.	10
			(PART B)	
3a	CO2	K2	What are assembler directives? explain any two directives.	10
3b	CO2	K2	Explain the operation of stack with an example.	10
			(OR)	
4a	CO2	K2	Explain the functions to be performed by a typical I/O interface with a typical input or output interface.	10
4b	CO2	K4	Aanlyze and Write a program to evaluate the arithmetic statement **Y=(a+b)*(c+d)** using three-address,two-address,one-address and zero address instructions	10
			(PART C)	

5a	CO3	K3	With neat sketches,explain the flowchart for I/O services routine.	10
			(OR)	
5b	CO3	K3	With neat sketches,Explain the Single Level Interrupt System.	10